Please replace the paragraph beginning at page 7, line 17, with the following rewritten paragraph:

Fig. 5 is a schematic illustration of a modified version of the digital converter of Fig. 3, according to an embodiment of the present invention.

Please replace the paragraph beginning at page 8, line 6, with the following rewritten paragraph:

Reference is now made to Fig. 1, which is a schematic illustration of a portion of an integrated circuit 100, having a DAC of an embodiment of the present invention implemented in it. Reference is made additionally to Fig. 2A, which is an exemplary graphical illustration of a pulse modulated signal as a function of time, and to Figs. 2B, 2C and 2D, which are exemplary graphical illustrations of the output analog signal of Fig. 1 as a function of time. In Figs. 2B, 2C and 2D, the horizontal line 201 indicates the desired constant analog signal.

Please replace the paragraph beginning at page 9, line 23, with the following rewritten paragraph:

According to an embodiment of the present invention, the DAC achieves a fast response time and a small ripple in the steady-state. When the multi-bit digital signal changes, resulting in a new single bit digital signal, the controller 106 closes switch SW1 and opens switch SW2 so that the capacitor C will charge in the fast response mode. This is shown in Fig. 2C by the solid-line graph 206. When the capacitor C reaches the desired voltage level at time T_1, the controller 106 opens switch SW1 and closes switch SW2 so that the capacitor C will retain its desired voltage level with a small ripple. This is shown in Fig. 2C by the dotted-line graph 208. In such a way, the DAC takes advantage of the fast response mode while the capacitor C is charging, and takes advantage of the small ripple mode when the capacitor C is close to or already at the desired voltage level. As a result, the DAC of the present invention produces a far more stable analog control signal than that of a conventional pulse modulated DAC.

Please replace the paragraph beginning at page 10, line 12, with the following rewritten paragraph:

A6 According to another embodiment of the invention, the DAC achieves a fast response time and no ripple in the steady-state. When the multi-bit digital signal changes, resulting in a new single bit digital signal, the controller 106 closes switch SW1 and opens switch SW2 so that the capacitor C will charge in the fast response mode. This is shown in Fig. 2D by the solid-line graph 210. When the capacitor C reaches the desired voltage level at time T_1, the controller 106 opens switch SW1 and closes switch SW2 so that the capacitor C will retain its desired voltage level with a small ripple. This is shown in Fig. 2D by the dotted-line graph 212. When a no-ripple, very stable analog signal is required at beginning at time T_3, the controller 106 opens both switches SW1 and SW2 so that the capacitor C will retain its voltage level in hold mode. This is shown in Fig. 2D by the almost flat dashed line 214.

Please replace the paragraph beginning at page 10, line 24, with the following rewritten paragraph:

A7 The motivation for this embodiment is that there are cases, such as control signals for time division multiple access (TDMA) applications, where a very stable, slowly decreasing signal is preferable to even a small ripple. In such applications, the controller is set so that the time T_3 precedes or substantially coincides with the time at which the analog control signal is needed.

Please replace the paragraph beginning at page 11, line 5, with the following rewritten paragraph:

A8 A further advantage of this embodiment is that during hold mode, the switchable LPF 104 draws no current, and the digital converter 102 can be turned off, resulting in a reduction in the overall power consumption.

Please replace the paragraph beginning at page 11, line 10, with the following rewritten paragraph:

The operation of the digital converter 102 of Fig. 1 will now be explained with respect to Figs. 3 and 4, to which reference is now made. Fig. 3 is a schematic illustration of a pulse density modulation (PDM) digital converter, according to an embodiment of the present invention.

Please replace the paragraph beginning at page 11, line 24, with the following rewritten paragraph:

According to a further embodiment of the present invention, the DAC spreads the spectral properties of the harmonic ripple using random noise. As is known in the art, a PDM signal is composed of pulses whose density is proportional to the value of the multi-bit digital input signal. The frequency of these pulses, known as the ripple frequency, appears in the output analog signal and interferes with the desired signal. The same problem occurs with the output analog signal of a PWM signal, although its ripple frequency is generally lower than that generated by a PDM signal. In this embodiment of the present invention, the timing of the pulses in the pulse modulated signal is adjusted by a small, random factor, thereby spreading the spectral properties of the harmonic ripple. Reference is now made additionally to Fig. 5, which is a schematic illustration of a modified version of the digital converter of Fig. 3, according to a further embodiment of the present invention. In addition to the adder 302 and the flip-flop 304, the digital converter 102 comprises a uniform distribution random number generator 500 and an additional adder 502. The random number generator 500, for example a pseudo-random number (PN) generator, which is known in the art, is driven by a clock 504. For each cycle of the clock 504, the random number generator 500 generates a random number in the range –M to +M, where M is significantly smaller than N. The adder 502 adds the random number to the value in the flip-flop 304, and the result is added by the adder 302 to the N-bit digital signal input. The resulting pulse modulated signal is shown in Fig. 4 by the dashed-line graph. The effect is that the pulses generated by the digital converter of Fig. 5 are slightly offset in time ("jittered") from the pulses generated by the digital converter of Fig. 3. Sometimes, as in pulse 400, the two signals are coincident, sometimes, as in pulse 402, the